**Unit: 1**

1. The number of bits used to store a BCD digit is: 4
2. The hexadecimal equivalent of the binary number 1011010 is : 5A
3. What is the resultant binary of the decimal problem 39 + 1 = ? : 00101000
4. The weight of the LSB as a binary number is: 1
5. What is difference binary coding and BCD? : Binary coding is purely binary
6. What is the decimal value of the hexadecimal number 333?: 819
7. Convert the binary number 1001.0010 to decimal: 9.125
8. Base 10 refers to which number system?: Decimal
9. The representation of number -7 using 1's complement system is given : 1001
10. 1248 is the decimal value for which of the following binary coded decimal: 0001001001001000
11. The gray code for binary number 10101 is : 11111
12. The octal equivalent of binary number 111011 is : 73
13. Sum of BCD number 10010000 and 10001000 is given as : 101111000
14. The binary equivalent of hexadecimal number 1A is given as : 00011010
15. the decimal equivalent of sum of binary numbers 100101 and 11101 is given as : 70
16. The octal representation of sum of two octal number 36 and 57 is given as: 115
17. The weight of the LSB as a hexadecimal number is: ans 1
18. The hexadecimal equivalent of octal number 123 is given as: 53
19. Base 16 refers to which number system? Hexadecimal
20. The decimal value of BCD number 0011 0100 0010 1000 is : 3428
21. The Excess-3 code for BCD number 1001 is given as: 1100
22. The representation of -2 using 2's complement system is given as: 1110
23. The sum of two binary numbers 10010 and 10110 is: 101000
24. The decimal equivalent of BCD number 101000 is : 28
25. The hexadecimal sum of two number 1A and AE is given as : C8
26. The difference of two binary numbers 111001-110001 is : 1000

2. The subtraction of a binary number Y from another binary number X, done by adding the 2’s complement of Y to X, results in a binary number without overflow. This implies that the result is:

(a) negative and is in normal form

(b) negative and is in 2’s complement form

(c) positive and is in normal form

(d) positive and is in 2’s complement form

3. The number of bits in ASCII is

(a) 12 (b) 10 (c) 9 (d) 7

4. The number of bits in EBCDIC is

(a) 12 (b) 10 (c) 8 (d) 6

5. (FF)16 when converted to 8421 BCD is

(a) 0000 0101 0101 (b) 0010 0101 0101

(c) 1111 0101 0101 (d) 1000 0101 0101

6. Decimal number 9 in Gray code is

(a) 1100 (b) 1101 (c) 110 (d) 1111

7. 11011 in gray code equal to binary

(a) (10010) (b) (11111) (c) (11100) (d) (10001)

8. The Gray code for decimal number 6 is equivalent to

(A) 1100 (B) 1001 (C) 0101 (D) 0110

9. The code where all successive numbers differ from their preceding number by single bit is

(A) Binary code. (B) BCD. (C) Excess – 3. (D) Gray.

10. -8 is equal to signed binary number

(A) 10001000 (B) 00001000 (C) 10000000 (D) 11000000

11. 1’s complement representation of decimal number of -17 by using 8 bit representation is

(A) 1110 1110 (B) 1101 1101 (C) 1100 1100 (D) 0001 0001

12. The excess 3 code of decimal number 26 is

(A) 0100 1001 (B) 01011001 (C) 1000 1001 (D) 01001101

13. The chief reason why digital computers use complemented subtraction is that it

(A) Simplifies the circuitry. (B) Is a very simple process.

(C) Can handle negative numbers easily. (D) Avoids direct subtraction.

14. The excess-3 code of decimal 7 is represented by

(A) 1100. (B) 1001. (C) 1011. (D) 1010.

15. The result of adding hexadecimal number A6 to 3A is

(A) DD. (B) E0. (C) F0. (D) EF.

1. Consider the operation 24 + 17 = 40. Find the correct base of number so that the operation is correct?

(a) 5 (b) 10 (c) 11 (d) 12

2. Find F’s complement of (2BFD)16.

(a) D402 (b) D505 (c) 13402 (d) none of these

3. -24 is 2’s complement form is

(a) 11101000 (b) 01001000

(c) 01111111 (d) 00111111

4. An equivalent 2’s complement representation of the 2’s complement number 1101 is

(a) 110100 (b) 001101 (c) 110111 (d) 111101

5. The 2’s complement representation of – 17 is

(a) 101110 (b) 101111 (c) 111110 (d) 110001

6. 4-bit 2’s complement representation of a decimal number is 1000. The number is

(a) +8 (b) 0 (c) -7 (d) -8

7. The range of signed decimal number that can be represented by 6-bit 1’s complement number is

(a) -31 to +31 (b) -63 to +63 (c) -64 to +63 (d) -32 to 31

8. 2’s complement representation of a 16-bit number (one sign bit and 15 magnitude bits) if FFFF. Its magnitude in decimal representation is

(a) 0 (b) 1 (c) 32, 767 (d) 65, 535

9. -8 is equal to signed binary number (8 bit)

(a) 10001000 (b) 00001000 (c) 1000000 (d) 11000000

10. 1’ s complement of 11100110 is

(a) 00011001 (b) 10000001 (c) 00011010 (d) 00000000

11. 2’s complement of binary number 0101 is

(a) 1011 (b) 1111 (c) 1101 (d) 1110

12. -8 is equal to signed binary number

(A) 10001000 (B) 00001000 (C) 10000000 (D) 11000000

13. 1’s complement representation of decimal number of -17 by using 8 bit representation is

(A) 1110 1110 (B) 1101 1101 (C) 1100 1100 (D) 0001 0001

14. In a positive logic system, logic state 1 corresponds to

(A) positive voltage (B) higher voltage level (C) zero voltage level (D) lower voltage level

15. The result of adding hexadecimal number A6 to 3A is (A) DD. (B) E0. (C) F0. (D) EF.

16. One hex digit is sometimes referred to as a(n):

(a) Byte (b) nibble (c) grouping (d) instruction

17. Which is typically the longest: bit, byte, nibble, word?

(a) Byte (b) nibble (c) bit (d) word

19. The most commonly used system for representing signed binary numbers is the:

(a) Two’s complement system (b) One’s complement system (c) Ten’s complement ststem(d) Nine’s complement system

20. Add the following hex numbers: 011016 + 1001016 (a) 10120 (b) 10020 (c) 11120 (d) 00120

21. Determine the two's-complement of each binary number. 00110 00011 11101

A. 11001 11100 00010 B. 00111 00010 00010 C. 00110 00011 11101 D. 11010 11101 00011

22. Solve this binary problem: 01110010 – 01001000 =

A. 00011010 B. 00101010 C. 01110010 D. 00111100

23. Solve this binary problem: 1000 – 0001 (a) 1001 (b) 0110 (c) 0111 (d) 0101

24. Perform the following hex subtraction: ACE16 – 99916 =

(a) (235)16 (b) (135)16 (c) (035)16 (d) (335)16

25. Solve this binary problem: 01101110 + 00100010

(a) 11001001 (b) 10010000 (c) 01101110 (d) 01110110

26. The number 1000 would appear just immediately after-

(a) FFFF (hex) (b) 1111(binary) (c) 7777(octal) (d) all of the above

28. (3104)x = (404)10 Then the value of x will be – (a) 4 (b) 5 (c) 6 (d) 7

29. (23)x = (19)10 Then the value of x will be – (b) 4 (b) 5 (c) 8 (d) 7

30. (0.8)x = (0.5)10 Then the value of x will be – (c) 4 (b) 8 (c) 16 (d) 20

Que.1 Find 10s complement of decimal number 4069.

(a)5930 (b) 5931 (c) 9604 (d) 5391

Que.2 Convert binary number 11011.101 into decimal

(a)26.625 (b) 111.10 (c) 27.625 (d) 33.5

Que. 3 Convert decimal number 163.875 into binary

(a)10100011.111 (b) 110100011.111 (c) 10100011.101 (d) 10100111.111

Que. 4 Perform binary subtraction 111.111 from 1010.01

(a)0010.011 (b) 1010.011 (c) 001.011 (d)101.110

Que. 5 Representation of decimal number -51 in 2s complement form is

(a)0110011 (b) 1110011 (c) 1001101 (d) 1001100

Que. 6 Equivalent value of binary number 10111 in 1s complement form is

(a)-7 (b) -9 (c) -8 (d) +23

Que. 7 Express decimal number -45 in 8 bit 2s complement form

(a)00101101 (b) 11010010 (c) 11010011 (d) 10100011

Que. 8 The number of bits required to assign binary roll numbers to a class of 60 students is

(a)5 (b) 6 (c) 7 (d) 8

Que. 9 The value of base if number 121 with base r is equal to 144 with base 8.

(a)7 (b) 6 (c) 8 (d) 9

Que. 10 A group of 8 bits is known as

(a) a nibble (b) a byte (c) a bit (d) an octal number

Que. 11 When two n bit binary numbers are added, the sum will contain at the most

(a) n bits (b) n+1 bits (c) n+2 bits (d) n+n bits

Que. 12 The highest decimal number that can be represented with 10 binary digits is

(a)512 (b) 1023 (c) 1024 (d) 2048

Que. 13 Represent decimal number 25 in 8421 code

(a) 00011001 (b) 00100101 (c) 01010010 (d) 00010110

Que. 14 Convert the binary 1001 into Gray code

(a)1001 (b) 1101 (c) 1011 (d) 1110

Que. 15 Convert the Gray code 1101 to binary.

(a)1001 (b) 1101 (c) 1011 (d) 1110

Que. 16 In an even parity scheme, which one is having error.

(a)10110001 (b) 1111101 (c) 101010111 (d) 111011011

Que. 17 The codes in which each successive code word differs from the preceding one in only one bit position are called

(a)BCD Code (b) Sequential Codes (c) Self complementing Codes (d) Cyclic Codes

Ans: 1 to 17

B C A A C C C B D B

B B B B A D D

Que. 18 A logic circuit that provides a HIGH output for both inputs HIGH or both inputs LOW is a(n):

(a)Ex-NOR Gate (b) OR Gate (c) Ex- OR Gate (d) NAND Gate

Que. 19 A logic circuit that provides a LOW output for both inputs HIGH or both inputs LOW is a(n):

(a)Ex-NOR Gate (b) OR Gate (c) Ex- OR Gate (d) NAND Gate

Que. 20 A logic circuit that provides a HIGH output only if both inputs LOW.

(a)Ex-NOR Gate (b) OR Gate (c) Ex- OR Gate (d) NAND Gate

Que. 21 Identify the type of gate below from the equation

(a)Ex-NOR Gate (b) OR Gate (c) Ex- OR Gate (d) NAND Gate

Que. 22 Identify the type of gate below from the equation

(a)Ex-NOR Gate (b) OR Gate (c) Ex- OR Gate (d) NAND Gate

Que.23 Which type of gate can be used to add two bits?

(a)Ex-NOR Gate (b) NOR Gate (c) Ex- OR Gate (d) NAND Gate

Que.24 If a gate is having a LOW into one of the inputs, and output is HIGH is a(n):

(a)AND Gate (b) OR Gate (c) NOR Gate (d) NAND Gate

Que. 25 Find the equivalent decimal numbers of binary number (110101)

(a) 53 (b) 45 (c) 55 (d) 65

Que. 26 Find the equivalent decimal numbers of binary number (101101)

(a) 18 (b) 45 (c) 55 (d) 65

Que. 27 Determine the equivalent decimal numbers of binary number (1100.1011)

(a) C.B (b) 14.54 (c) 12.687 (d) 12.54

Que. 28 Express the decimal number (25.5) in binary form

(a)11001.1 (b) 11100.01 (c) 00110.0 (d) 011001.01

Que. 29 Express the decimal number (0.6875) in binary form

(a)1.011 (b) 0.1010 (c) 0.1011 (d) 1.1011

Que. 30 Represent decimal number (-15) in one’s complement form

(a) 10000 (b) 01111 (c) 100000 (d) 010000

Que. 31 Find two’s complement of the binary number (01100111)

(a) 10011000 (b) 01101000 (c) 10011001 (d) 11100111

Que. 32 Add the binary number 1011 and 1100

(a)0111 (b) 10111 (c) 10100 (d) 1000

Que. 33 Add the binary number 0101 and 1111

(a)0111 (b) 10111 (c) 10100 (d) 1000

Que. 34 Perform binary subtraction where minuend is 1011 and subtrahend is 0110

(a) 0101 (b) 1010 (c) 1011 (d) 1101

Que. 35 Multiply 1001 by 1101

(a) 1110101 (b) 110101 (c) 1101101 (d) 0001010

36. Which of the following is minimum error code?

[A] Octal code

[B] Grey code

[C] Binary code

[D] Excess 3 code

37. Radix of binary number system is \_\_\_\_\_?

[A] 0

[B] 1

[C] 2

[D] A & B

38. The output of an AND gate is LOW \_\_\_\_\_\_\_\_.

[A] when any input is LOW

[B] all the time

[C] when all inputs are HIGH

[D] when any input is HIGH

39. Which of the following statements does NOT describe an advantage of digital technology?

[A] The values may vary over a continuous range.

[B] The circuits are less affected by noise.

[C] The operation can be programmed.

[D] Information storage is easy.

Ans: 18 to 39

A C D C A A D A B C A C A C B C A A B C A A

Q40. The universal gate is ………………

1. NAND gate
2. OR gate
3. AND gate
4. None of the above

Q41. The inverter is ……………

1. NOT gate
2. OR gate
3. AND gate
4. None of the above

Q42. The inputs of a NAND gate are connected together. The resulting circuit is ………….

1. OR gate
2. AND gate
3. NOT gate
4. None of the above

Q43. Digital circuit can be made by the repeated use of ………………

1. OR gates
2. NOT gates
3. NAND gates
4. None of the above

Q44. The only function of NOT gate is to ……………..

1. Stop signal
2. Invert input signal
3. Act as a universal gate
4. None of the above

Q45. When an input signal 1 is applied to a NOT gate, the output is ………………

1. 0
2. 1
3. Either 0 & 1
4. None of the above

46. The Gray code for decimal number 6 is equivalent to

(A) 1100 (B) 1001

(C) 0101 (D) 0110

47. The hexadecimal number ‘A0’ has the decimal value equivalent to

(A) 80 (B) 256

(C) 100 (D) 160

48. The code where all successive numbers differ from their preceding number by single bit is

(A) Binary code. (B) BCD.

(C) Excess – 3. (D) Gray.

49. What is the binary equivalent of the decimal number 368

(A) 101110000 (B) 110110000

(C) 111010000 (D) 111100000

50. The decimal equivalent of hex number 1A53 is

(A) 6793 (B) 6739

(C) 6973 (D) 6379

51. The output of a logic gate is 1 when all its inputs are at logic 0. the gate is either

(A) a NAND or an EX-OR (B) an OR or an EX-NOR

(C) an AND or an EX-OR (D) a NOR or an EX-NOR

52. -8 is equal to signed binary number

(A) 10001000 (B) 00001000

(C) 10000000 (D) 11000000

53. 1’s complement representation of decimal number of -17 by using 8 bit representation is

(A) 1110 1110 (B) 1101 1101

(C) 1100 1100 (D) 0001 0001

54. The excess 3 code of decimal number 26 is

(A) 0100 1001 (B) 01011001

(C) 1000 1001 (D) 01001101

Ans: 40 to 54

1 1 3 3 2 1 C C D A B D A A D

1. The number system with radix 2 is known as –

(a) Binary (b) Octal (c) Decimal (d) Hexadecimal

2. A group of 8 bits is known as –

(a) A nibble (b) A byte (c) A bit (d) none of these

3. The radix for hexadecimal number system will be-

(a) 2 (b) 4 (c) 8 (d) 16

4. Knowledge of binary number system is required by designers of computers because-

(a) It is easy to learn binary number system

(b) It is easy to learn Boolean algebra

(c) It is easy to use binary codes

(d) The devices used in these systems operate in a binary manner

5. The binary equivalent of hexadecimal number AOB5 is-

(a) 0101111010110101

(b) 0101111110110101

(c) 1010000010110101

(d) 1011000011000101

6. The binary equivalent of the octal number 362 is-

(a) 011110010

(b) 101110010

(c) 011101010

(d) None of these

7. Binary equivalent if decimal number 0.0625 is –

(a) 1001110001

(b) 0.1001110001

(c) 0.0110001110

(d) 0.0001

8. A group of 4 bits is known as –

(a) A nibble (b) A byte (c) A bit (d) none of these

9. Hexadecimal number system is used in digital computers and digital systems to-

(a) Perform arithmetic operations

(b) Input binary data into systems

(c) Perform logical operations

(d) Perform arithmetic and logical operations

10. Octal equivalent of decimal number 41 is –

(a) 61 (b) 51 (c) 41 (d) none of these

11. 1’ s complement of 11100110 is

(a) 00011001 (b) 10000001 (c) 00011010 (d) 00000000

12. 2’s complement of binary number 0101 is

(a) 1011 (b) 1111 (c) 1101 (d) 1110

13. (E7F6)16 = (-----)10

(a) (600000)10 (b) (59382)10 (c) (9382)10 (d) (382)10

14. Two voltages are 0V and -5V. In positive logic –

(a) 0V is 1 and -5V is 0

(b) -5V is 1 and 0V is 0

(c) 0V is 1 in some circuit and 0 in others

(d) -5V is 1 in some circuit and 0 in others

15. The number FF in hexadecimal system has equivalence in decimal system to

(a) 256 (b) 255 (c) 240 (d) 239

16. (268)10 = (----)16

(a) 10A (b) 10B (c) 10C (d) 10D

17. MSD stands for-

(a) Most significant digit (b) Many significant digit (c) Both a and b (d) None

18. The number that immediately follow (1111)2 is -

(a) (1000)2 (b) (11111)2 (c) (11110)2 (d) None of these

19. Which numbering system uses numbers and letters as symbols ?

(a) decimal (b) binary (c) octal (d) hexadecimal

20. The number that come immediately after hex number (FFEF)16 is –

(a) (FFF0)16 (b) (FFFE)16 (c) (FFEE)16 (d) None of these

21. Consider the operation 24 + 17 = 40. Find the correct base of number so that the operation is correct?

(a) 11 (b) 9 (c) 8 (d) 5

22. (7BF)16 = (----)2

(a) 0111 1011 1110 (b) 0111 1011 1111

(c) 0111 1011 0111 (d) 0111 1011 0011

23. What is the binary equivalent of the decimal number 368 –

(A) 101110000 (B) 110110000 (C) 111010000 (D) 111100000

24. (734)8 = ()16

(A) C 1 D (B) D C 1 (C) 1 C D (D) 1 D C

25. The 2’s complement of the number 1101101 is-

(A) 0101110 (B) 0111110 (C) 0110010 (D) 0010011

26. 1’s complement representation of decimal number of 17 is -

(A) 01110 (B) 11101 (C) 01100 (D) 01000

27. The hexadecimal number for ( 95.5 )10 is –

(A) (5F.8 )16 (B) ( 9A.B)16 (C) (2E.F)16 (D) ( 5A.4)16

28. In a positive logic system, logic state 1 corresponds to –

(A) positive voltage (B) higher voltage level (C) zero voltage level (D) lower voltage level

29. How many address bits are required to represent a 32 K memory

(A) 10 bits.(B) 12 bits.(C) 14 bits. (D) 16 bits

30. The 2’s complement of the number 1101110 is-

(A) 0010001. (B) 0010001. (C) 0010010. (D) None

31. How many address bits are required to represent 4K memory

(A) 5 bits.(B) 12 bits.(C) 8 bits.(D) 10 bits.

32. Which of the following memories stores the most number of bits –

(A) 64K x 8 memory. (B) 1M x 8 memory (C) 32M × 8 memory. (D) 64 × 6 memory.

33. A bulb in a staircases has two switches, one switch being at the ground floor and the other one at the first floor. The bulb can be turned ON and also can be turned OFF by and one of the switches irrespective of the state of the other switch. The logic of switching of the bulb resembles.

(a) an AND gate (b) an OR gate (c) an XOR gate (d) a NAND gate

34. The digit F in hexadecimal system has equivalence in digital system to-

(a) 16 (b) 15 (c) 17 (d) 18

35. 1’ s complement of 01100111 is- (a) 10011000 (b) 10000001 (c) 00011010 (d) 00000000

**Unit: 2**

The code used for labeling cells of the K Map is

(a) BCD (b) Hexadecimal (c) Gray (d) Octal

Ans: C

The number of cells in a 6 variable K-Map is

(a) 6 (b)12 (c) 36 (d) 64

Ans: D

Each term in the standard SOP form is called a

(a) minterm (b) maxterm (c) donot care (d) literal

Ans: A

Each term in the standard POS form is called a

(a) minterm (b) maxterm (c) donot care (d) literal

Ans: B

The binary number designation of the rows and columns of the K Map are in

(a) binary code (b) BCD code (c) Gray code (d) Excess 3 code

Ans: C

An 8 square eliminates

(a) 2 variables (b) 3 variables (c) 4 variables (d) 8 variables

Ans: B

An 4 square eliminates

(a) 2 variables (b) 3 variables (c) 4 variables (d) 8 variables

Ans: A

An 8 square is called

(a) Pair (b) Quad (c) Octet (d) Cube

Ans: C

An 4 square is called

(a) Pair (b) Quad (c) Octet (d) Cube

Ans: B

The minimum number of 2 input NAND gate required to realize a half adder is

(a) 4 (b) 5 (c) 6 (d) 7

Ans: B

The minimum number of 2 input NAND gate required to realize a half substractor is

(a) 4 (b) 5 (c) 6 (d) 7

Ans: B

The logic gate used in parity generator is

(a) AND (b) NAND (c) Ex OR (d) NOR

Ans: C

A BCD to decimal decoder is

(a) a 3 to 8 decoder (b) a 1 to 10 decoder (c) a 4 to 8 decoder (d) a 8 to 3 decoder

Ans: C

Which of the following expressions is in the sum-of-products (SOP) form?

[A] AB + CD

[B] AB(CD)

[C] (A + B)(C + D)

[D] (A)B(CD)

Ans: A

When simplified with Boolean Algebra (x + y)(x + z) simplifies to

(A) x (B) x + x(y + z)

(C) x(1 + yz) (D) x + yz

Ans: D

|  |
| --- |
| Which of the following expressions is in the product-of-sums form? |
| |  |  | | --- | --- | | [A.](javascript:%20void%200;) | (A + B)(C + D) | | [B.](javascript:%20void%200;) | (AB)(CD) | | [C.](javascript:%20void%200;) | AB(CD) | | [D.](javascript:%20void%200;) | AB + CD |   Answer: Option A |

How many AND gates are required to realize Y = CD+EF+G

(A) 4 (B) 5 (C) 3 (D) 2

Ans: D

How many two-input AND and OR gates are required to realize Y=CD+EF+G

(A) 2,2 (B) 2,3 (C) 3,3 (D) none of these

Ans: A

The gates required to build a half adder are

(A) EX-OR gate and NOR gate (B) EX-OR gate and OR gate

(C) EX-OR gate and AND gate (D) Four NAND gates.

Ans: C

Q.83 A full adder logic circuit will have

(A) Two inputs and one output.

(B) Three inputs and three outputs.

(C) Two inputs and two outputs.

(D) Three inputs and two outputs.

Ans: D

The number of control lines for a 8 to 1 multiplexer is

(A) 2 (B) 3 (C) 4 (D) 5

Ans: B

When the set of input data to an even parity generator is 0111, the output will be

(A) 1 (B) 0 (C) Unpredictable (D) Depends on the previous input

Ans: B

A universal logic gate is one, which can be used to generate any logic function. Which of the following is a universal logic gate?

(A) OR (B) AND (C) XOR (D) NAND

Ans: D

Karnaugh map is used for the purpose of

(A) Reducing the electronic circuits used.

(B) To map the given Boolean logic function.

(C) To minimize the terms in a Boolean expression.

(D) To maximize the terms of a given a Boolean expression.

Ans: C

Which of following are known as universal gates

(A) NAND & NOR. (B) AND & OR.

(C) XOR & OR. (D) None.

Ans: A

NOR function is dual of

1. AND function
2. OR function
3. XOR function
4. NAND function

D

Dual of NAND function is

1. AND function
2. OR function
3. NOR function
4. NAND function

C

Most basic arithmetic function is

1. Addition
2. Subtraction
3. Multiplication
4. Division

A

Circuits whose output depends on directly present input is called

1. combinational circuit
2. sequential circuit
3. combinational sequence
4. series

A

Full substractor is a

1. combinational circuit
2. sequential circuit
3. combinational sequence
4. series

A

Two bit addition is done by

1. ripple carry adder
2. carry sum adder
3. full adder
4. half adder

D

In map dont cares input are marked by

1. 0
2. 1
3. star
4. X

D

Full adder performs addition on

1. 2 bits
2. 3 bits
3. 4 bits
4. 5 bits

B

Result of two bit subtract or is called

Difference bit Least significant bit Most significant bit Carry bit

A

Borrow in two bit (x,y) subtraction is 0, as long as

1. y>x
2. x=y
3. x>=y
4. y>=x

C

In real design procedure we consider

1. max no of gates
2. min no of gates
3. two gates
4. three gates

B

Combinational circuits are described by

1. Boolean functions
2. algebric functions
3. geometric functions
4. linear equations

A

|  |  |
| --- | --- |
|  | How many data select lines are required for selecting eight inputs? |
| |  |  | | --- | --- | | [A.](javascript:%20void%200;) | 1 | | [B.](javascript:%20void%200;) | 2 | | [C.](javascript:%20void%200;) | 3 | | [D.](javascript:%20void%200;) | 4 | |

C

|  |  |
| --- | --- |
|  | Which of the following combinations cannot be combined into K-map groups? |
| |  |  | | --- | --- | |  | Corners in the same row | |  | Corners in the same column | |  | Diagonal corners | |  | Overlapping combinations |   Answer: Option C |

|  |
| --- |
| Which gate is best used as a basic comparator? |
| |  |  | | --- | --- | |  | NOR | |  | OR | |  | Exclusive-OR | |  | AND |   Answer: Option C |
|  |
|
| The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels? |
| |  |  | | --- | --- | | [A.](javascript:%20void%200;) | A > B = 1, A < B = 0, A < B = 1 | | [B.](javascript:%20void%200;) | A > B = 0, A < B = 1, A = B = 0 | | [C.](javascript:%20void%200;) | A > B = 1, A < B = 0, A = B = 0 | | [D.](javascript:%20void%200;) | A > B = 0, A < B = 1, A = B = 1 |   Answer: Option C |

|  |
| --- |
| Looping on a K-map always results in the elimination of: |
| |  |  | | --- | --- | |  | Variables within the loop that appear only in their complemented form. | |  | Variables that remain unchanged within the loop. | |  | Variables within the loop that appear in both complemented and uncomplemented form. | |  | Variables within the loop that appear only in their uncomplemented form. |   Answer: Option C |

|  |
| --- |
| A decoder can be used as a demultiplexer by \_\_\_\_\_\_\_\_. |
| |  |  | | --- | --- | |  | Tying all enable pins LOW | |  | Tying all data-select lines LOW | |  | Tying all data-select lines HIGH | |  | Using the input lines for data selection and an enable line for data input |   Answer: Option D |

|  |
| --- |
| Which statement below best describes a Karnaugh map? |
| |  |  | | --- | --- | | [A.](javascript:%20void%200;) | A Karnaugh map can be used to replace Boolean rules. | | [B.](javascript:%20void%200;) | The Karnaugh map eliminates the need for using NAND and NOR gates. | | [C.](javascript:%20void%200;) | Variable complements can be eliminated by using Karnaugh maps. | | [D.](javascript:%20void%200;) | Karnaugh maps provide a visual approach to simplifying Boolean expressions. |   Answer: Option D |

|  |  |
| --- | --- |
| When adding an even parity bit to the code 110010, the result is \_\_\_\_\_\_\_\_. | |
| [A.](javascript:%20void%200;) | 1110010 |
| [B.](javascript:%20void%200;) | 1111001 |
| [C.](javascript:%20void%200;) | 110010 |
| [D.](javascript:%20void%200;) | 001101 |

Answer: Option A

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. Select one of the following statements that best describes the parity method of error detection: Parity checking is best suited for detecting single-bit errors in transmitted codes. 2. Most demultiplexers facilitate which of the following? Single input, multiple outputs 3. How many inputs are required for a 1-of-10 BCD decoder? 4 4. One application of a digital multiplexer is to facilitate: Parallel to serial data conversion 5. Number of NOR gates required to realize an AND gate is : 3 6. A NAND gate has: LOW inputs and a HIGH output 7. How many NAND circuits are contained in a 7400 NAND IC? : 4 8. How many truth table entries are necessary for a four-input circuit? : 16 9. Exclusive-OR (XOR) logic gates can be constructed from what other logic gates: And, OR and not 10. The basic logic gate whose output is the complement of the input is: Not 11. Which statement below best describes a Karnaugh map?: Re-arranged Truth table 12. Which of the examples below expresses the distributive law of Boolean algebra   Ans: A (B + C) = (AB) + (A C)   1. The output will be a LOW for any case when one or more inputs are zero in a(n): AND gate 2. Select an Universal gate from the following: NAND 3. Which digital system translates coded characters into a more intelligible form?: Decoder 4. Number of NAND gates required to realize an OR gate is : 3 5. How many truth table entries are necessary for a five input circuit?: 32 6. XOR logic gates can be constructed from what other logic gates?: AND gates, OR gates, and NOT gates 7. What input values will cause an OR logic gate to produce a Low output? All inputs low 8. What input values will cause a XOR logic gate to produce a Low?: All Inputs Same. 9. In an IC 7402 how many Nor gates are present? : 2 10. The sum output of a full adder can be expressed as: Xor of all inputs 11. Which of the examples below expresses the commutative law of multiplication?: AB=BA 12. For a 4-variable Karnaugh map number of cells required are: 16 13. Identify the basic gates from the following : And, OR, Not 14. The output will be a HIGH for any case when one or more inputs are zero in a(n): Nand   **Unit: 3**  The most popular DAC is  (a) R 2R ladder type (b) weighted resistor type (c) switched current source type (d) flash type  Ans: A  The simplest type ADC is  (a) counter type (b)successive approximation type (c) dual slope type (d) flash type  Ans: A  The most widely used ADC is  (a) counter type (b)successive approximation type (c) dual slope type (d) flash type  Ans: B  The ADC which has fixed conversion time is  (a) counter type (b)successive approximation type (c) dual slope type (d) flash type  Ans: B  In which ADC, conversion time depends on the magnitude of the analog input is  (a) counter type (b)successive approximation type (c) dual slope type (d) flash type  Ans: A   |  | | --- | | Why must CMOS devices be handled with care? | | |  |  | | --- | --- | |  | so they don’t get dirty | |  | because they break easily | |  | because they can be damaged by static electricity discharge  None of these |   Answer: Option C |  |  | | --- | | What should be done to unused inputs on TTL gates? | | |  |  | | --- | --- | |  | They should be left disconnected so as not to produce a load on any of the other circuits and to minimize power loading on the voltage source. | |  | All unused gates should be connected together and tied to Vcc through a 1 k ohm resistor. | |  | All unused inputs should be connected to an unused output; this will ensure compatible loading on both the unused inputs and unused outputs. | |  | Unused AND and NAND inputs should be tied to VCC through a 1 k ohm resistor; unused OR and NOR inputs should be grounded. |   Answer: Option D | | PMOS and NMOS \_\_\_\_\_\_\_\_. | | |  |  | | --- | --- | |  | represent MOSFET devices utilizing either P-channel or N-channel devices exclusively within a given gate | |  | are enhancement-type CMOS devices used to produce a series of high-speed logic known as 74HC | |  | represent positive and negative MOS-type devices, which can be operated from differential power supplies and are compatible with operational amplifiers | |  | None of the above |   Answer: Option A |   The digital logic family which has minimum power dissipation is  (A) TTL (B) RTL  (C) DTL (D) CMOS  Ans: D  Which of the following is the fastest logic  (A) TTL (B) ECL  (C) CMOS (D) LSI  Ans: B  The digital logic family which has the lowest propagation delay time is  (A) ECL (B) TTL  (C) CMOS (D) PMOS  Ans: A  CMOS circuits consume power  (A) Equal to TTL (B) Less than TTL  (C) Twice of TTL (D) Thrice of TTL  Ans: B  CMOS circuits are extensively used for ON-chip computers mainly because of their extremely  (A) low power dissipation. (B) high noise immunity.  (C) large packing density. (D) low cost.  Ans: C  Which of following consume minimum power  (A) TTL. (B) CMOS.  (C) DTL. (D) RTL.  Ans: B   |  | | --- | | Which of the following logic families has the shortest propagation delay? | | |  |  | | --- | --- | |  | CMOS | |  | BiCMOS | |  | ECL | |  | 74SXX |   Answer: Option C | |  | |
| What is the major advantage of ECL logic? |
| |  |  | | --- | --- | |  | very high speed | |  | wide range of operating voltage | |  | very low cost | |  | very high power |   Answer: Option A |

|  |
| --- |
| What is the range of invalid TTL output voltage? |
| |  |  | | --- | --- | | [A.](javascript:%20void%200;) | 0.0–0.4 V | | [B.](javascript:%20void%200;) | 0.4–2.4 V | | [C.](javascript:%20void%200;) | 2.4–5.0 V | | [D.](javascript:%20void%200;) | 0.0–5.0 V |   Answer: Option B |

|  |
| --- |
|  |
|  |
| Q. No.1 :-Why must CMOS devices be handled with care? |
| |  |  | | --- | --- | | [A](javascript:%20void%200;)) | so they don’t get dirty | | [B](javascript:%20void%200;)) | because they break easily | | [C](javascript:%20void%200;)) | because they can be damaged by static electricity discharge | |

D) None of above

Ans:- C

|  |
| --- |
| Q. No. 2:-Which of the following logic families has the shortest propagation delay? |
| |  |  | | --- | --- | | A) | CMOS | | B) | BiCMOS | | C) | |  |  | | --- | --- | | ECL |  | | | D) | 74SXX | |

Ans:- C

Q. No. 2:- A family of logic devices designed for extremely high speed applications is called

A) NMOS.

B) ECL.

C) PMOS.

D) TTL.

Ans:- B

Q. No. 3:-The number of total steps of a 9-bit ADC is,

A) 255

B) 256

C) 511

D) 512.

Ans. C

|  |
| --- |
| Q. No. 3:- Which logic family combines the advantages of CMOS and TTL? |
| |  |  | | --- | --- | | [A](javascript:%20void%200;)) | BiCMOS | | [B](javascript:%20void%200;)) | TTL/CMOS | | [C](javascript:%20void%200;)) | ECL | | [D](javascript:%20void%200;)) | TTL/MOS | |

Ans:- A

|  |
| --- |
| Q. No. 4:- Which equation is correct? |
| |  |  | | --- | --- | | [A](javascript:%20void%200;)) | VNL = VIL(max) + VOL(max) | | [B](javascript:%20void%200;)) | VNH = VOH(min) + VIH(min) | | [C](javascript:%20void%200;)) | VNL = VOH(min) – VIH(min) | | [D](javascript:%20void%200;)) | VNH = VOH(min) – VIH(min) | |

Ans:- D

Q. No. 4:-Which equation is correct?

A. VNL = VIL(max) – VOL(max)

B. VNL = VIL(min) – VOL(min)

C. VNH = VIH(min) + VOH(min)

D. VNH = VIL(max) – VOL(max)

Ans:- A

Q. No. 5:- What is the resolution of a digital-to-Analog converter (DAC)?

A. It is the deviation between the ideal straight-line output and the actual output of the converter.

B. It is the smallest analog output change that can occur as a result of an increment in the digital input.

C. It is the comparison between the actual output of the converter and its expected output.

D. It is its ability to resolve between forward and reverse steps when sequenced over its entire range.

Ans:- B

Q. No. 5:- The difference between analog voltage represented by two adjacent digital codes, or the analog step size, is the:

A. Quantization

B. Accuracy

C. Resolution

D. monotonicity

Ans:- C

#### Q. No. 6:-What is the major advantage of the R/2R ladder digital-to-analog (DAC), as compared to a binary-weighted digital-to-analog DAC converter?

A. It only uses two different resistor values

B. It has fewer parts for the same number of inputs.

C. Its operation is much easier to analyse.

D. The virtual ground is eliminated and the circuit is therefore easier to understand and troubleshoot.

Ans:- A

#### Q. No. 6:- What is the disadvantage of binary weighted type DAC?

A.Require wide range of resistors.

B. High operating frequency.

C. High power consumption.

D. Slow switching

Ans:- A

Q. No. 7:-Which one of the following is odd?

A). Multiplexer

B). Decoder

C). Adder

D). Flip-Flop

Q. No. 7:- When the binary input is all zeros, ideally the output of a DAC will be?

A) Zero volt

B) Full scale output voltage

C) 1 volt

D) One step voltage.

Ans. A

Q. No. 8:- As compared to TTL, ECL has

A. Lower power dissipation

B. Lower propagation delay

C. Higher propagation delay

D. Higher noise margin

Ans:-B

Q. No. 8:-As compared to TTL CMOS logic has

A. Higher speed of operation

B. Higher power dissipation

C. Smaller physical size

D. All the above

Ans:- C

Q. No. 9:- A common means for comparing the propagation delays and the power dissipation of various logic gates is the

A) Fan-out.

B) Power requirements.

C) Speed-power product.

D) Noise margin.

Ans:- C

Q. No. 9:-Each digital input of DAC are weighted according to their position in the

A) Binary number.

B) Decimal number.

C) Hexa-decimal number.

D) Octal number.

Ans:- A

Q.No. 10:-Which logic family has the highest power dissipation per gate

A. ECL

B. TTL

C. CMOS

D. PMOS

Ans:- a

Q.No. 10:- One advantage that MOSFET transistors have over bipolar transistors is

A) reduced propagation delay.

B) higher switching speed.

C) high input impedance.

D) low input impedance.

Ans:- C

Q.No.11:-Resolution of DAC is equal to the weight of

A) LSB

B) MSB

C) full scale output

D) 1 volt.

Ans. A

Q.No.11:- Which is the most commonly used logic family

A. ECL

B. TTL

C. CMOS

D. PMOS

Ans:- B

Q.No.12:- The full forms of the abbreviations TTL and CMOS in reference to logic families are

A. Triple Transistor Logic and Chip Metal Oxide Semiconductor

B. Tristate Transistor Logic and Chip Metal Oxide Semiconductor

C. Transistor Transistor Logic and Complementary Metal Oxide Semiconductor

D. Tristate Transistor Logic and Complementary Metal Oxide Silicon

Ans:- C

Q.No.12:-The full forms of the abbreviations RTL and ECL in reference to logic families are

A. Resistor Transistor Logic and Emitter Collector Logic

B. Resistor Transistor Logic and Emitter Coupled Logic

C. Resistor Transmission Logic and Emitter Collector Logic

D. Resistor Transmission Logic and Emitter Coupled Logic

Ans:- B

Q.No.13:- Which of the following is a concern when using CMOS type devices?

A). mechanical shock

B). electrostatic discharge

C). fan out

D).under voltage

Ans:- B

Q.No.13:-The number of gates that can be connected to a single output without exceeding the current ratings of the gate is called

A) Dissipation.

B) Propagation.

C) Fan-out.

D) SSI.

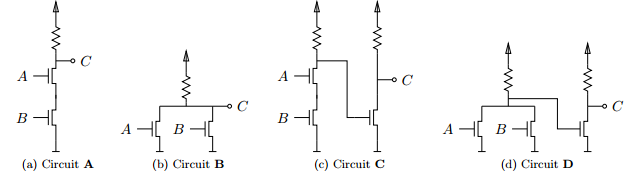
Ans:- C

Q.No.14:- This gate is equivalent to

B

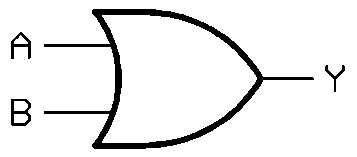
A

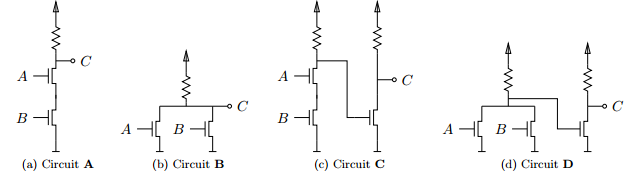
C



Ans:- C

Q.No.14:- This gate is equivalent to





Ans:- D

Q. No.1 :- Which of the following digital IC logic families is most susceptible to static discharge?

A) RTL

B) ECL

C) MOS

D) TTL

Ans:- C

1. ECl stands for { Emitter Coupled Logic}
2. Out of TTL and Cmos which has lower noise margin: TTL
3. For an ideal logic family fanout should be: High
4. ULSI stands for: { Ultra Large Scale Integration}
5. Which of the following is an example of DAC?{ R-2R Ladder}
6. Which of the following{TTL/ CMos} has minimum propagation delay?: TTL
7. From the following, the logic family with a high Power dissipation: TTL
8. The maximum number of digital inputs that the output of a single logic gate can feed is known as: Fanout
9. Which of the following logic families has the Largest fanout?: CMOS
10. Which of the following are DAC? R-2R Ladder, Weighted type
11. Out of SAR and Counter type ADC converters, the fastest is: SAR
12. An LSI device has a circuit complexity of: 10,000 to 99,999 equivalent gates
13. TTL is made with: Bipolar Junction Transistor
14. CMOS is made from: c. field effect transistor
15. VLSI refers to digital ICs having: More than 100 but less than 9999
16. Logic families which are in use now a days are: TTL, ECL and CMOS
17. As compared to TTL, CMOS has: Lower power dissipation
18. ADC stands for:
19. What is the resolution of a digital-to-analog converter (DAC)?: It is the smallest analog output change that can occur as a result of an increment in the digital input.
20. The full forms of the abbreviations TTL and CMOS in reference to logic families are: Transistor Transistor Logic and Complementary Metal Oxide Semiconductor
21. Time delay of a TTL standard family is above: 10ns
22. TTL uses: Multiemitter Transistor
23. Which of the following{CMos and TTL} logic families has the smallest fanout?: TTL
24. Which of the following{ Counter type Converter & R-2R ladder} is an Analog to digital converter? Counter type Converter
25. MOS stands for: {Metal Oxide Semiconductor}.
26. A digital voltmeter contains a(n): ADC
27. RTL stands for: Resistor Transistor Logic
28. LSI stands for : Large Scale Integration

The Gray code for binary number 01101 is

1. 11001
2. 01011
3. 01101
4. 10001

Answer B

The Gray code for binary number 1001 is

1. 1101
2. 0101
3. 0110
4. 1000

Answer A

Number 225 in BCD code is given by

1. 111011011010
2. 001000100101
3. 000100100101
4. 111011011011

Answer B

Number 597 in BCD code is given by

1. 111011011010
2. 001000100111
3. 000100100111
4. 010110010111

Answer D

The Excess-3 code is a

1. error correcting code
2. self- complementing code
3. cyclic code
4. none of the above

Answer B

The Excess-3 code of binary number (11011) 2  is

1. 11110
2. 10110
3. 11001
4. 00011

Answer A

The value of base r if (121)r = (144)8 is

1. 7
2. 8
3. 9
4. 10

Answer C

If (292)10 = (204)b , the possible base b is

1. 8
2. 12
3. 14
4. 16

Answer B

A group of 8 bits is known as

1. a nibble
2. a byte
3. a bit
4. an octal number

Answer B

BCD code is not a

1. XS-3 code
2. 8421 Code
3. Gray code
4. Binary coded decimal code

Answer C

Convert a given gray code (11011010) Gray to binary

1. 10010011
2. 11001001
3. 10011011
4. 10010111

Answer A

In positive logic the high voltage level of a digital signal is

1. 0
2. 1
3. either 0 or 1
4. none of the above

Answer b

Binary 1111 when subtracted from binary 11111, the result in binary is given by

1. 1111
2. 1000
3. 10000
4. 111111

Answer C

The result of binary 1111 when added to binary 11111 is

1. 100010
2. 101110
3. 10110
4. 10000

Answer B

The decimal form of binary 0.0111 is given by

1. 0.4375
2. 0.7964
3. 0.2728
4. 0.1600

Answer a

The decimal equivalent of the binary 1111111 is

1. 167
2. 127
3. 87
4. 67

Answer B

The incorrect binary addition is

1. 11111 + 10001 = 110000
2. 11111 + 11111 = 100000
3. 10101 + 10011 = 101000
4. 1001 + 1101 = 10110

Answer B

The incorrect binary product is

1. 1.01 X 10.1 = 11.001
2. 1100 X 1010 = 1111000
3. 1100110 X 1000 = 1100110000
4. None of above

Answer D

The 10’s complement of decimal 1932 is

1. 8806
2. 8608
3. 8068
4. 8868

Answer C

Decimal equivalent of octal 16 is given by

1. 15
2. 16
3. 13
4. 14

Answer D

The equivalent octal number of the decimal number 545.375 is

1. 1041.3
2. 1170.7
3. 5141
4. 1644

Answer A

The hexadecimal number for the binary number 0.01111110 is given by

1. 0.5E
2. 0.7F
3. 0.9E
4. 0.6E

Answer B

The octal number for the binary number 101101 is

1. 51
2. 65
3. 45
4. 55

Answer D

The 2’s complement for the binary number 11011.01 is

1. 01111.10
2. 00100.11
3. 0101.110
4. 01100.10

Answer B

Digital signals are

1. Continuous
2. discrete
3. ‘0’ only
4. ‘1’ only

Answer B

Analog signals are

1. ‘0’ and ‘1’ only
2. Discrete
3. Continuous
4. None of the above

Answer C

A NOT gate has…

a. Two inputs and one output

b. One input and one output

c. One input and two outputs

d. none of above

Answer B

An OR gate has…

a. Two inputs and one output

b. One input and one output

c. One input and two outputs

d. none of above

Answer A

The output of a logic gate can be one of two \_\_\_\_\_?

a. Inputs

b. Gates

c.States

d. none of the above

Answer A

The output of a \_\_\_\_ gate is only 1 when all of its inputs are 1

a. NOR

b. XOR

c. AND

d. NOT

answer C

A NAND gate is equivalent to an AND gate plus a …. gate put together.

a. NOR

b. NOT

c. XOR

d. none

Answer B

Half adder circuit is \_\_\_\_\_\_?

a. Half of an AND gate

b. A circuit to add two bits together

c. Half of a NAND gate

d. none of above

Answer B

The NAND gate can function as a NOT gate if

1. all inputs are connected together
2. inputs are left open
3. one input is set to 0
4. one input is set to 1

Answer A

The NOR gate can function as a NOT gate if

1. all inputs are connected together
2. inputs are left open
3. one input is set to 0
4. one input is set to 1

Answer A

An X-OR gate gives a high output

1. if there are odd number of 1’s
2. if it has even number of 0’s
3. if the decimal value of digital word is even
4. for odd decimal value

Answer A

The X-OR and X-NOR gates can have how many inputs?

1. 2
2. 1
3. 4
4. any number

Answer A

What logic function is produced by adding inverters to the inputs of an AND gate ?

1. OR
2. NOR
3. NAND
4. X-OR

Answer B

What logic function is produced by adding inverters to the inputs of an OR gate ?

1. OR
2. NOR
3. NAND
4. X-OR

Answer C

A bubbled NAND gate is equivalent to a

1. OR
2. NOR
3. NAND
4. X-OR

Answer A

A bubbled NOR gate is equivalent to a

1. OR
2. AND
3. NAND
4. X-OR

Answer B

A + B = B + A ; AB = BA represent which laws ?

1. Commutative
2. Associative
3. Distributive
4. Idempotence

Answer A

( A + B ) + C = A + ( B + C ) ; (AB) C = A(BC) represent which laws ?

1. Commutative
2. Associative
3. Distributive
4. Idempotence

Answer B

A + AB = A ; A(A +B) = A represent which laws ?

1. Commutative
2. Associative
3. Absorption
4. Idempotence

Answer C

The logic expression F = AB + B’C + AC is an

1. SOP Form
2. POS Form
3. standard SOP Form
4. standard POS Form

Answer A

The logic expression F = (A+B+C) (A+C’)(B+C’)(A+C) is an

1. SOP Form
2. POS Form
3. standard SOP Form
4. standard POS Form

Answer B

Each term in the standard SOP form is called a

1. minterm
2. maxterm
3. don’t care
4. literal

Answer A

Each term in the standard POS form is called a

1. minterm
2. maxterm
3. don’t care
4. literal

Answer B

An n variable K-map can have

1. n2 cells
2. 2n cells
3. nn cells
4. n2n cells

Answer B

How many inputs and outputs does a full adder have ?

1. two inputs, two outputs
2. two inputs, one output
3. three inputs, two outputs
4. two inputs, three outputs

Answer C

How many inputs and outputs does a full subtractor have ?

1. two inputs, two outputs
2. two inputs, one output
3. three inputs, two outputs
4. two inputs, three outputs

Answer C

A full adder can be realized using

1. one half adder, two OR gates
2. two half adder, one OR gates
3. two half adder, two OR gates
4. two half adder, one AND gates

Answer B

A multiplexer is also known as

1. a data accumulator
2. a data restorer
3. a data selector
4. a data distributor

Answer C

The most popular and most widely used IC family is

1. TTL
2. IIL
3. MOS
4. CMOS

Answer A

The TTL circuit acts as a current sink in the

1. low state
2. high state
3. high impedance state
4. none of these

Answer A

The TTL circuit acts as a current source in the

1. low state
2. high state
3. high impedance state
4. none of these

Answer B

The TTL series most suitable at high frequencies is

1. standard TTL
2. Schottky TTL
3. FTTL
4. Low power TTL

Answer C

The fastest saturated logic family is

1. TTL
2. ECL
3. IIL
4. MOS

Answer A

The fastest logic family is

1. TTL
2. ECL
3. IIL
4. MOS

Answer B

Noise margin of a TTL gate is given by

1. 0.4V
2. 0.6V
3. 0.8v
4. 0.2V

Answer A

The logic family preferred in superfast computers is

1. TTL
2. ECL
3. IIL
4. MOS

Answer B

The IC’s used in watches and calculators are of

1. TTL
2. ECL
3. MOS
4. CMOS

Answer D

The slowest logic family is

1. TTL
2. IIL
3. MOS
4. CMOS

Answer C

The parameters which are not specified for digital IC’s

1. propagation delay
2. noise margin
3. bandwidth
4. gate dissipation

Answer C

The logic family which has the highest fan-out is

1. TTL
2. IIL
3. MOS
4. CMOS

Answer D

The logic family which has the highest noise margin is

1. TTL
2. IIL
3. MOS
4. CMOS

Answer D

The logic family most suitable for SSI and MSI is

1. TTL
2. IIL
3. MOS
4. CMOS

Answer A

The number of inputs the gate is designed to handle is called

1. Fan – out
2. Fan – in
3. Noise margin
4. none of these

Answer B

The LSI chip contains

1. More than 500 but less than 1000 gates
2. More than 100 gates
3. More than 5000 gates
4. More than 100 but less than 1000 gates

Answer D

The logic family which consumes least power is

1. TTL
2. ECL
3. MOS
4. CMOS

Answer D

The number of subfamilies TTL has is

1. 4
2. 8
3. 6
4. 10

Answer B

For TTL Logic, which of the characteristics mentioned below is not true

1. High cost
2. Good Speed
3. Low power dissipation per gate
4. None of the above

Answer A

The logic family which is simplest to fabricate is

1. TTL
2. ECL
3. MOS
4. CMOS

Answer C

The logic family ideally suited for LSI/VLSI/ULSI application is

1. TTL
2. ECL
3. MOS
4. CMOS

Answer C

The newest of the logic families is the

1. TTL
2. ECL
3. IIL
4. CMOS

Answer C

The most popular DAC is

1. R-2R ladder type
2. weighted resistor type
3. switched current source type
4. switched capacitor type

Answer A

The simplest type of ADC is

1. counter- type
2. flash type
3. successive –approximation type
4. dual-slope type

Answer A

The fastest ADC is

1. counter- type
2. flash type
3. successive –approximation type
4. dual-slope type

Answer B

The most expensive ADC is

1. counter- type
2. flash type
3. successive –approximation type
4. dual-slope type

Answer B

The slowest ADC is

1. counter- type
2. flash type
3. successive –approximation type
4. dual-slope type

Answer D

The most widely used type of ADC is

1. counter- type
2. flash type
3. successive –approximation type
4. dual-slope type

Answer C